ResearchGate

See discussions, stats, and author profiles for this publication at: https://www.researchgate.net/publication/306913803

Comparative analysis of differential colpitts and cross-coupled VCOs in 180 nm Si-Ge HBT technology

Conference Paper · May 2016

DOI: 10.1109/ISCAS.2016.7538883

CITATION
1

READS
110

4 authors:

Macera Giuseppe
Analog Devices, Inc.
12 PUBLICATIONS 5 CITATIONS

SEE PROFILE

Michael Peter Kennedy
University College Dublin
270 PUBLICATIONS 7,452 CITATIONS

SEE PROFILE

E. Napoli
University of Naples Federico II
136 PUBLICATIONS 1,436 CITATIONS

SEE PROFILE

Valerio Marotta
University College Cork
5 PUBLICATIONS 6 CITATIONS

SEE PROFILE

Some of the authors of this publication are also working on these related projects:

Modeling and design of SuperJunction (SJ) devices View project

Local lifetime control for high speed low loss power devices View project

All content following this page was uploaded by Michael Peter Kennedy on 15 September 2017.

The user has requested enhancement of the downloaded file.

Comparative Analysis of Differential Colpitts and Cross-Coupled VCOs in 180 nm Si-Ge HBT Technology

Valerio Marotta[1,2] Giuseppe Macera[1,2] Michael Peter Kennedy[2,3,4] Ettore Napoli[1]

[1]Università degli Studi di Napoli Federico II
Naples, ITALY

[2]Tyndall National Institute
Cork, IRELAND

[3]School of Engineering—Electrical and Electronic Engineering
University College Cork
Cork, IRELAND

[4]Microelectronic Circuits Centre Ireland
Tyndall National Institute
Cork, IRELAND

***Abstract*—It has been shown in the literature that a cross-coupled CMOS LC VCO will outperform an equivalent Colpitts VCO. In the case of bipolar devices, the jury is still out. This paper reports a comparative analysis of phase noise (PN), tuning range (TR), dissipated DC power and Figure of Merit (FoM) in cross-coupled and differential Colpitts LC VCOs topologies designed in 180 nm Si-Ge HBT technology for operation around 5 GHz. SpectreRF simulations show that the cross-coupled topology exhibits a minimum PN equal to -108 dBc/Hz, a tuning range of 17.5% and a dissipated DC power of 12.6 mW, with a FoM equal to 204 dB, while the Colpitts topology exhibits a minimum PN over the tuning range equal to -113 dBc/Hz, a tuning range of 21.6% and a dissipated DC power of 14.1 mW, with a FoM equal to 212 dB. This suggests that, for the considered technology, the differential Colpitts can exhibit better overall performance than the cross-coupled VCO.**

I. Introduction

One of the most critical components in radio-frequency communication systems is the voltage-controlled oscillator (VCO), which is used as a local oscillator to up- and downconvert signals, and is a fundamental part of phase-locked loops, clock recovery circuits and frequency synthesizers. Due to the ever-increasing demand for bandwidth, very stringent requirements are placed on the spectral purity of local oscillators. In the GSM 900 standard, for example, the PN power per unit bandwidth must be about 165 dB below the carrier power (i.e., -165 dBc/Hz) at an offset of 20 MHz. Also, the large demand for low-power portable battery-operated electronic devices makes the dissipated DC power a key parameter when considering the performance of a VCO.

The Colpitts architecture has long been used in its single-ended configuration [1] but, as the number of transistors is no longer a key cost factor, a differential version has also been developed. By virtue of symmetry, differential topologies are ideally immune to common-mode noise, such as that coming from the supply rails or from the bias network. In several works [2]–[4], these topologies have been analyzed in CMOS technology. The conclusion [4], [5] is that the CMOS cross-coupled oscillator outperforms its differential Colpits counterpart.

There are a number of reasons to expect that the situation might be different in the case of Si-Ge HBT technology [6]. In particular,

- Si-Ge HBT devices have a much lower flicker noise corner compared to CMOS [6]; and
- the cutoff frequency f_T of a Si-Ge HBT is very high with respect to a standard BJT.

Furthermore, the reduced base width decreases the base resistance r_b and increases the Early voltage V_A. In addition, the junction capacitance C_{je} is also reduced. All these features contribute to oscillator PN, so exploiting the advantages of Si-Ge HBT technology in VCO topologies could provide interesting results.

In some of the latest published work, the cross-coupled oscillator is presented as the better choice in CMOS technology [7], while in others which consider only Si-Ge HBT technology, the Colpitts is deemed the better option [8]. In this work, we compare the differential Colpitts and cross-coupled topologies in a Si-Ge HBT technology in terms of Phase Noise, Tuning Range, Dissipated Power and Figure of Merit (FoM). The two oscillator topologies have been analyzed under the same common design conditions, including DC power consumption, supply voltage, transistor sizing, inductance and quality factor of the integrated spiral inductors, MOS varactor, and considering the full models of the transistors available within the PDK, including all their parasitic components, but excluding the layout interconnections.

The VCOs are optimized for phase noise at an offset frequency of 100 kHz, since they are intended for use in a high performance point-to-point wireless communication system. In fact, to obtain good PN performance at this frequency offset, BJT technology is the better option, due to the fact that MOSFETs have a much higher flicker noise corner frequency.

This paper is organized as follows: in Sec. II, the design and the characteristics of the circuit topologies are described; Sec. III reports the performance of the two topologies. Finally, we present our conclusions in Sec. IV.

II. VCO Circuit Topologies

Two architectures have been designed and simulated in 180 nm Si-Ge HBT technology, with a 3.3 V supply (V_{cc}).

A. Cross-coupled VCO

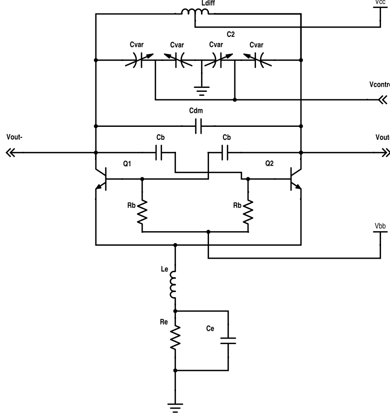


Fig. 1. Cross-coupled topology.

In the core of the cross-coupled LC VCO topology shown in Fig. 1, a differential inductor is used, with the center tap connected to the supply. A capacitor C_{dm} sets the center frequency. The variable capacitors are implemented using accumulation-mode MOS varactors, as they offer better performance in terms of tuning range and PN with respect to reverse biased diode varactors [9]. Moreover, a back-to-back series varactor configuration is used, because it is a suitable solution to reduce the amplitude to phase noise conversion with respect to the conventional topology [10]. The tail current is implemented with a resistor R_e instead of a transistor source, to avoid the $1/f$ noise component [4]. The capacitor C_e, inductor L_e and resistor R_e together form a filter that shunts to ground the second harmonic noise component [7]. Only salicided resistors and MIM capacitors between metal 1 and 2 were adopted. The topology used for the cross-coupled VCO is not a standard one, but uses a more suitable structure for a BJT-based implementation: the DC bias on the base of the transistors is necessary to prevent the transistors from entering the saturation region, and the capacitors C_b decouple the rest of the circuit from the bias [7]. All the components are taken from the sbc18 PDK library. The sizes of the active and passive devices used are reported in Table I, and the varactor and inductor sizing in Table II. The components are chosen for a center frequency of 5 GHz. The inductor's size has been chosen to have the highest Q available in the PDK at 5 GHz.

The VCO has been designed for class-C operation, since it provides a larger oscillation amplitude and lower phase noise using less current [11]. Futhermore, care is taken to ensure that the BJTs are kept out of their saturation regions.

The oscillation frequency is given by

$$\omega_{osc,cross\text{-}coupled} \approx \frac{1}{\sqrt{L(2C_A + C_B)}}, \tag{1}$$

TABLE I
Cross-coupled device sizing

Active devices	Value	Passive devices	Value
$Emitter\ Length$	8.7 μm	Re	580 Ω
$Emitter\ Width$	0.5 μm	R_b	490 Ω
$Multiplier$	10	C_b	400 fF
$EBC\ Fingers$	232	C_{dm}	130 fF
$Emitter\ Metal$	M2	C_e	560 fF
		L_e	0.4 nH

TABLE II
Varactor and Inductor sizing

Varactor	Value	Inductor	Value
$Width$	4 μm	$Outer\ dimension$	300 μm
$Length$	0.48 μm	$Width$	34 μm
$Fingers$	10	$Spacing$	2 μm
$Slices$	10	$Number\ of\ turns$	2
$Multiplier$	1	$Operating\ frequency$	5 GHz
C_{min}	720.82 fF	$Inductance\ value$	0.58 nH
C_{max}	1.91 pF	$Q\ factor$	23.86

where

$$C_A = \frac{2C_\mu C_b}{C_\mu + C_b}, \quad C_B = 2(C_{dm} + C_{var}). \tag{2}$$

C_μ is the base-collector capacitance of the transistor. Cadence simulations match the predicted frequency to within 5%.

B. Differential Colpitts VCO

The common-base differential Colpitts topology shown in Fig. 2 has the same differential inductor and varactors as the cross-coupled circuit. For the bias network, consisting of R_{b1}, R_{b2} and R_e, a second 3 V supply is used (V_{bb}). The capacitive voltage divider of the Colpitts topology is realized with the two capacitors C_1 and C_2. The two capacitors C_b on the bases of the transistors act as decoupling capacitors, and serve also to minimize frequency pushing by the base voltage [12].

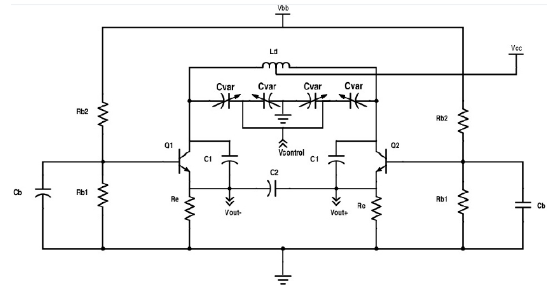


Fig. 2. Differential Colpitts topology.

The sizes of the active and passive devices used are reported in Table III, with the varactor and inductor sizing in Table II, as before. Once again, the VCO has been designed for class-C operation, and care has been taken to ensure that the BJTs are kept out of their saturation regions.

In this case,

$$\omega_{osc,Colpitts} \approx \frac{1}{\sqrt{L(2C_A + C_B)}}, \tag{3}$$

TABLE III
COLPITTS DEVICE SIZING

Active devices	Value	Passive devices	Value
$Emitter\ Length$	8.7 μm	Re	367.5 Ω
$Emitter\ Width$	0.5 μm	R_{b1}	15.2 kΩ
$Multiplier$	10	R_{b2}	15 kΩ
$EBC\ Fingers$	232	C_b	600 pF
$Emitter\ Metal$	M2	C_1	900 fF
		C_2	800 fF

where

$$C_A = \frac{C_1(C_2 + C_\mu) + C_2(C_{cs} + C_{var})}{C_1 + 2C_2 + C_\pi} \quad (4)$$

and

$$C_B = \frac{C_1 C_\pi + (C_1 + C_\pi)(C_{cs} + C_\mu + C_{var})}{C_1 + 2C_2 + C_\pi}. \quad (5)$$

Here, C_π is the base-emitter capacitance and C_{cs} is the collector to substrate capacitance. Once again, Cadence simulations match the predicted frequency to within 5%.

III. PERFORMANCE COMPARISON

Fig. 3 reports the PN obtained through the Semi-Empirical Leeson's model described in [13], [14], and the PN calculated through Periodic Steady State (PSS) and Periodic Noise (PNoise) in Spectre-RF. In general, the theoretical prediction of the semi-empirical Leeson's model is expected to differ by 2–5 dB from Spectre-RF simulations, which compute the Floquet modes for autonomous circuits [15] for the PN calculation. Despite this descrepancy, Leeson's equation allows us to quickly predict by hand the expected PN, so it is a powerful method to determine which topology offers a lower PN.

The Semi-Empirical Leeson's equation is [14]:

$$L\{\Delta\omega\} = 10 \log \left\{ \frac{2FkT}{P_{sig}} \left[1 + \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \right] \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|} \right) \right\}. \quad (6)$$

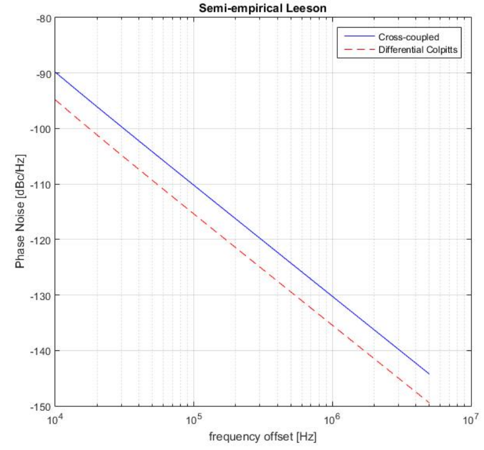
Table IV compares the two topologies in terms of the minimum PN over the Tuning Range, calculated by means of Spectre-RF and with the Semi-Empirical Leeson's model (S-E Leeson), at 100 kHz frequency offset. As we can see, the discrepancy between Leeson's model and Spectre-RF falls within the range of 2 to 5 dB, but the differential Colpitts has lower phase noise in both theory and simulation.

TABLE IV
PN @100 KHZ OFFSET FREQUENCY [*dBc/Hz*]

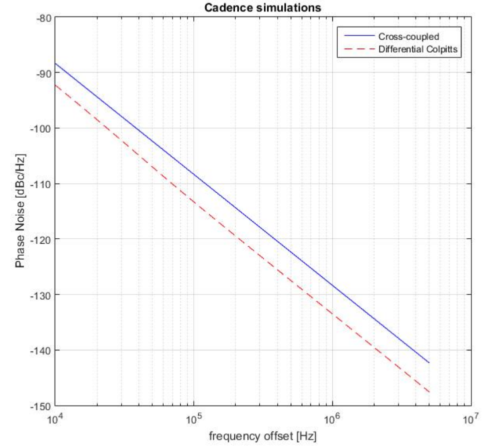
Topology	PN Spectre-RF	PN S-E Leeson
$Cross\text{-}coupled$	-108.36	-110.4
$Colpitts$	-113.37	-115.4

Table V shows the noise contributions from the active and passive devices. The main contribution comes from the transistors and is thermal. The flicker noise corner frequencies of the two topologies are 1.02 kHz for the cross-coupled and 1.59 kHz for the differential Colpitts topologies, respectively. This confirms that a BJT technology is more suitable than CMOS if we seek better PN performance at small offsets. While the MOSFET flicker noise corner frequency is in the order of MHz [16], for the BJTs in this PDK the flicker noise corner frequency is in the order of kHz.

The dissipated DC power in the two topologies is roughly the same, respectively 12.6 mW for the cross-coupled, and 14.1 mW for the Colpitts. The tuning range is 17.5% for the cross-coupled, within the range of 4.53 GHz to 5.43 GHz, and 21.6% for the differential Colpitts, within the range of 4.29 GHz to 5.33 GHz.



(a)



(b)

Fig. 3. PN predicted by (a) the semi-empirical Leeson's model and (b) Cadence simulations.

TABLE V
PN CONTRIBUTIONS [*% of total*]

Device	Cross-coupled	Diff. Colpitts
$I_c(Q_{1,2})$	58.97	53.5
$r_b(Q_{1,2})$	1.5	5.42
$r_c(Q_{1,2})$	0.74	1.0
Inductor L_{diff}	22.23	24.14
Varactors C_{var}	6.54	5.94
R_e	0.59	6.53
R_b	3.24	
$r_{sub}(Q_{1,2})$		0.98

TABLE VI
STATE OF THE ART

Year	Ref	Type	Technology	f_{osc} (GHz)	TR (GHz)	PN (dBc/Hz)	P_{DC} (mW)	FoM_T (dB)	Results
2005	[8]	Differential Colpitts	SiGe HBT	5	0.2	-108 @100kHz	n/a	n/a	meas
2014	[17]	Class-C	CMOS 55nm	7.15	1.3	-127 @1MHz	18	206	meas
2005	[18].1	Cross-coupled	CMOS 180 nm	5.15	1.5	-88 @100kHz	1.2	200	sim
2005	[18].2	Cross-coupled	CMOS 180 nm	5.3	1.2	-81 @100kHz	0.9	193	sim
2005	[19]	Differential Colpitts	CMOS 180 nm	5	n/a	-120 @1MHz	n/a	189	meas
2013	[20]	Cross-coupled	CMOS 180 nm	4	1.91	-115 @1MHz	2.99	196	meas
2009	[21]	Quadrature Colpitts	CMOS 180 nm	5.44	0.25	-124 @1MHz	9.9	189	meas
This work		Differential Colpitts	Si-Ge 180 nm	4.85	1.04	-113.4 @100kHz	14.1	212.1	sim
		Cross-coupled	Si-Ge 180 nm	5	0.97	-108.4 @100kHz	12.5	204.3	sim

The tuning range based FoM (FoM_T) at an offset f_{off} from the carrier, is defined by:

$$FoM_T = 10\log_{10}\Big(\frac{Tuning\ Range^2}{P_{d,DC} \times L_{PN} \times f_{off}^2}\Big), \qquad (7)$$

where $Tuning\ Range$ is calculated as $f_{max}-f_{min}$, with f_{max} and f_{min} being the maximum and the minimum frequency of the VCO, $P_{d,DC}$ is the DC Dissipated Power from the VCO, L_{PN} is the Phase Noise at frequency offset f_{off}.

Table VII summarizes the comparative performance.

TABLE VII
PERFORMANCES SUMMARY (SPECTRERF)

Parameters	**Cross-coupled**	**Differential Colpitts**
$Phase\ Noise$	-108.4 dBc/Hz	-113.4 dBc/Hz
$P_{d,DC}$	12.6 mW	14.1 mW
$Tuning\ Range$	17.5%	21.6%
FoM_T	204.3 dB	212.1 dB

IV. CONCLUSIONS

In this paper, we have compared the *simulated* performance of cross-coupled and differential Colpitts VCOs designed in 180 nm Si-Ge HBT technology, operating at a center frequency of 5 GHz. The results show that, under roughly the same design conditions, the differential Colpitts topology considered in this study outperforms the cross-coupled VCO in terms of its overall performance. The original target was to obtain a PN lower than -110 dBc/Hz, and this was achieved with the differential Colpitts topology.

V. ACKNOWLEDGEMENT

Supported by Science Foundation Ireland grants 13/IA/1979 and 13/RC/2077, and by Enterprise Ireland grant CC-2009-05.

REFERENCES

[1] R. Saeidi, N. Msoumi, F. Kalantari, and M. S. Oskooei, "Analyzing of Phase Noise in CMOS LC Oscillators," *Microelectronics, 2005. ICM 2005. The 17th International Conference on*, pp. 330–337, 13-15 December 2005.

[2] I. Chlis, D. Pepe, and D. Zito, "Phase Noise comparative analysis of LC oscillators in 28-nm CMOS through the Impulse Sensitivity Function," *Ph.D. Research in Microelectronics and Electronics (PRIME), 2013 9th Conference on*, pp. 85–88, 24-27 June 2013.

[3] M. M. Mansour and M. M. Mansour, "On the design of low phase-noise CMOS LC-tank oscillators," *Microelectronics, 2008. ICM 2008. International Conference on*, pp. 407–412, 14-17 December 2008.

[4] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in colpitts and LC-tank CMOS oscillators," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 5, pp. 1107–1118, 2005.

[5] D. Murphy, H. Darabi, and H. Wu, "A VCO with Implicit Common-Mode Resonance," *Solid- State Circuits Conference - (ISSCC), 2015 IEEE International.*, pp. 1–3, 22-26 February 2015.

[6] J. D. Cressler, "SiGe HBT technology: a new contender for Si-based RF and microwave circuit applications," *Microwave Theory and Techniques, IEEE Transactions on.*, vol. 46, no. 5, pp. 572–589, 1998.

[7] P. Andreani, "Phase Noise in Harmonic Oscillators," Tutorial Lecture, ESSCIRC 2014, Venice, Italy, 22 September 2014.

[8] H. Zirath, R. Kozhuharov, and M. Ferndahl, "Balanced Colpitt Oscillator MMICs Designed for Ultra-Low Phase Noise," *Solid-State Circuits, IEEE Journal of.*, vol. 56, no. 12, pp. 2077–2086, October 2005.

[9] P. Andreani and S. Mattisson, "A 1.8-GHz CMOS VCO tuned by an accumulation-mode MOS varactor," *Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on.*, vol. 1, pp. 315–318, 28-31 May 2000.

[10] A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita, "A varactor configuration minimizing the amplitude-to-phase noise conversion in VCOs," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 53, no. 3, pp. 481–488, 2006.

[11] M. Tiebaut, "RF design in BiCMOS," *41st European Solid-State Circuit Conference: Messe Congress Graz, Austria.*, vol. 1, no. 2, pp. 1–116, 2015.

[12] R. Gilmore and L. Besser, *Practical RF Circuit Design for Modern Wireless Systems*. Artech House Boston, London, 2003, vol. II.

[13] B. Razavi, "A study of phase noise in CMOS oscillators," *Solid-State Circuits, IEEE Journal of.*, vol. 31, no. 3, pp. 331–343, 1996.

[14] T. H. Lee and A. Hajimiri, "Oscillator phase noise: a tutorial," *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 3, pp. 326–336, 2000.

[15] P. Maffezzoni, F. Pepe, and A. Bonfanti, "A Unified Method for the Analysis of Phase and Amplitude Noise in Electrical Oscillators," *Microwave Theory and Techniques, IEEE Transactions on.*, vol. 61, no. 9, pp. 3277–3284, 2013.

[16] I. Chlis, D. Pepe, and D. Zito, "Comparative Analyses of Phase Noise in Differential Oscillator Topologies in 28 nm CMOS Technology," *Ph.D. Research in Microelectronics and Electronics (PRIME), 2014 10th Conference on.*, pp. 1–4, 30 June - 3 July 2014.

[17] S. Perticaroli, S. Dal Toso, and F. Palma, "A Harmonic Class-C CMOS VCO-Based on Low Frequency Feedback Loop: Theoretical Analysis and Experimental Results," *IEEE Transactions on Circuit and Systems*, vol. 61, no. 9, pp. 2537–2549, 2014.

[18] C.-Y. Wu and C.-Y. Yu, "A 0.8V 5.9GHz Wide Tuning Range CMOS VCO using Inversion-Mode Bandswitching Varactors," *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on.*, vol. 5, pp. 5079–5082, 23-26 May 2005.

[19] M.-D. Tsai, Y.-H. Cho, and H. Wang, "A 5-GHz Low Phase Noise Differential Colpitts CMOS VCO," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 5, pp. 327–329, 2005.

[20] T.-P. W. S.-Y. Wang, "A Low-Voltage Low-Power Low-Phase-Noise Wide-Tuning-Range 0.18-μm CMOS VCO with High-Performance FOMT of -196.3 dBc/Hz," *Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International.*, pp. 1–4, 2-7 June 2013.

[21] S.-L. Jang, S.-H. Huang, C.-C. Liu, and M.-H. Juang, "CMOS Colpitts Quadrature VCO Using the Body Injection-Locked Coupling Technique," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 4, pp. 230–232, 2009.

View publication stats